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For
7/11 i52
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Primary

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CLAIMS

WHAT IS CLAIMED IS:

1.   A system, comprising:

a bus;

a memory coupled to the bus, wherein the memory includes a plurality of storage locations,

wherein the plurality of storage locations are divided into a plurality of memory units;

and

a device coupled to access the memory over the bus, wherein the device comprises:

one or more locks configured to control access to one or more of the plurality of

10   memory units; and

an access lock override register that stores one or more access lock override bits,

including a lock override bit:

wherein access to the one or more of the plurality of memory units is not allowed when the

lock override bit is set.

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2.   The system of claim 1. wherein the bus is configured to operate according to an LPC

bus protocol.

3.   The system of claim 1, wherein the memory is a ROM.

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4.   The system of claim 3, wherein the ROM is a BIOS ROM.

5.   The system of claim 1, wherein the device is a south bridge.